This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Previously Amended) A method for forming a semiconductor device, comprising:

etching a first portion of a dielectric layer formed on a semiconductor topography with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen and comprises C_4F_8; and

etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry, wherein the first and second etch chemistries are selective to silicon nitride.

2. (Original) The method of claim 1, wherein the dielectric layer is substantially continuous.

3. (Original) The method of claim 1, wherein an interface does not exist between the first and second portions of the dielectric layer.

4. (Original) The method of claim 1, wherein a thickness of the first portion of the dielectric layer is greater than a thickness of the second portion of the dielectric layer.

5. (Previously Amended) The method of claim 1, wherein the semiconductor topography comprises a gate structure formed on a semiconductor layer, and wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of the gate structure.

6. (Previously Canceled)

7. (Original) The method of claim 1, wherein the first etch chemistry further comprises CO.

8. (Original) The method of claim 1, wherein the second etch chemistry comprises at least one hydrogen-containing compound.

9. (Original) The method of claim 1, wherein the second etch chemistry comprises $C_2H_2F_4$.

10. (Original) The method of claim 1, wherein the second etch chemistry comprises CHF_3.

11. (Original) The method of claim 1, further comprising forming said dielectric layer on said semiconductor topography in one processing step.

12. (Original) The method of claim 1, wherein the first etch chemistry has a dielectric material: silicon nitride selectivity of at least approximately 10:1, and wherein the dielectric layer comprises the dielectric material.

13. (Original) The method of claim 1, wherein the second etch chemistry has a dielectric material: silicon oxide selectivity of at least approximately 5:1, and wherein the dielectric layer comprises the dielectric material.

14. (Original) The method of claim 1, wherein the dielectric layer comprises a doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. %.

15. (Original) The method of claim 1, wherein the semiconductor topography comprises a gate structure formed on a semiconductor layer, wherein the semiconductor layer comprises isolation regions, and wherein the dielectric layer is in contact with a sidewall spacer of the gate structure and the semiconductor layer.

16. (Original) The method of claim 15, wherein etching the first portion of the dielectric layer exposes an upper corner of the sidewall spacer, and wherein etching the second portion of the dielectric layer exposes the semiconductor layer.

17. - 18. (Canceled)

19. (Previously Canceled)

20. - 27. (Canceled)